Journal of Computer Applications ISSN: 0974 – 1925,
Volume-5, Issue EICA2012-5, February 10, 2012

FPGA Implementation of High Performance Face Detection Using MCT and Adaboost Algorithm

Ramya N
P.G.Scholar, ECE,
SKP Engineering College,
Tiruvannamalai India
E-mail : ramyamevlsi@gmail.com

Srimathi Mathiazhagan
Assistant Professor, ECE,
SKP Engineering College,
Tiruvannamalai, India

Abstract- In this paper, The proposed novel architecture and FPGA implementation is for high performance real time face detection engine for various illumination in mobile applications.MCT(modified census transform) and adaboost algorithms are the basic algorithms used for face detection engine. The hardware architecture of face detection engine is for high-performance face detection and real-time processing. We propose to implement a face detection chip through the FPGA`.The FPGA chip has advantage in real time processing, low power consumption, high performance and low cost. So this chip can perform better in mobile applications.

Keywords : *FPGA, MCT.*

I. INTRODUCTION

Face detection (human) plays an important role in applications such as human computer interface, face recognition video surveillance and face image database management. Face-detection systems carry out a major role in biometric authentication, which uses features of the face, iris, fingerprint, retina, etc. These systems are usually used in places requiring high security, such as government agencies, bank, and research institutes; it is also applied to two- or three- dimensional face detection in areas such as artificial intelligence and robots, access control systems, cutting-edge digital cameras and advanced vehicle systems. Recently, the face-detection technology is being adopted in the mobile phone applications because of the pros in easy installation, low-cost, non-contacting method. Most of the existing face- detection engines in digital camera or mobile phone have been run by software. However, the tendency is that the technology is being developed to be run by hardware for improving the processing speed. These days, the technology is to combine hardware technique of face-detection and software technique of emotion, feeling, physiognomy and fortune recognition.

Face detection performance is known to be highly influenced by variations in illumination. Especially in mobile environment, the illumination condition is dependent on the surroundings (indoor and outdoor), time, and light reflection, etc. The proposed face-detection method is designed to detect in the variable illumination conditions through the MCT techniques, which can reduce the effects of illumination by extracting the structural information of objects. The proposed face-detection engine also renders high performance face detection rate by extracting highly reliable and optimized learning data through the Adaboost learning algorithm.

II. BASIC ALGORITHMS

A. MCT (Modified Census Transform)

MCT presents the structural information of the window with the binary pattern {0, 1} moving the 3×3 window in an image small enough to assume that lightness value is almost constant, though the value is actually variable. This pattern contains information on the edges, contours, intersections, etc. MCT can be defined with the equation below:

$$(X) = \bigotimes_{Y \in N'} \zeta(\bar{I}(X), I(Y)) \qquad (1)$$

Here X represents a pixel in the image, the 3×3 window of which X is the center is W(X); N' is a set of pixels in W(X) and Y represents nine pixels each in the window. In addition, $\bar{I}(X)$ is the average value of pixels in the window, and $I(Y)$ is the brightness value of each pixel in the window. As a comparison function, $\zeta(\,)$ becomes 1 in the case of $\bar{I}(X) < I(Y)$, other cases are 0. As a set operator, $\bigotimes$ connects binary patterns of function, and then nine binary patterns are connected through operations. As a result, a total of 511 structures can be produced, as theoretically not all nine-pixel values can be 1. Thus connected binary patterns are transformed into binary numbers, which are the values of the pixels in MCT-transformed images.

B. Adaboost learning Algorithm

Adaboost learning algorithm is created high-reliable learning data as an early stage for face-detection using faces data. Viola and Jones [1] have proposed fast, high- performance face-detection algorithm. It is composed of cascade structure with 38 phases, using extracted features to effectively distinguish face and non-face areas through the Adaboost learning algorithm proposed by Freund and Schapire [2]. Furthermore, Froba and Ernst[3] have introduced MCT- transformed images and a face detector consisting of a cascade structure with 4 phases using the Adaboost learning algorithm.

This paper consists of a face detector with a single-layer structure, using only the fourth phase of the cascade structure proposed by Froba and Ernst.

III. PROPOSED HARDWARE STRUCTURE

Regarding proposed hardware structure as shown in Figure 1, it is composed of color conversion module to convert to gray image from color image, noise reduction module to reduce image noise, image scalar module to detect various size of the face, MCT transform module to transform image for robustness various illumination, CD (Candidate detector) / CM (Confidence mapper) to detect candidate for final face detection, position resizer module to resize face candidate areas detected on the scaled-down images as their corresponding points of original image size, data grouper module to group the duplicate areas determined to be the same face prior to determining the final face detection areas, overlay processor to play in displaying an output by marking square in relation to the final face-detection area on the color-based original image from the camera or to output to transfer the information of area and size in face-detection area to embedded system through host interface .

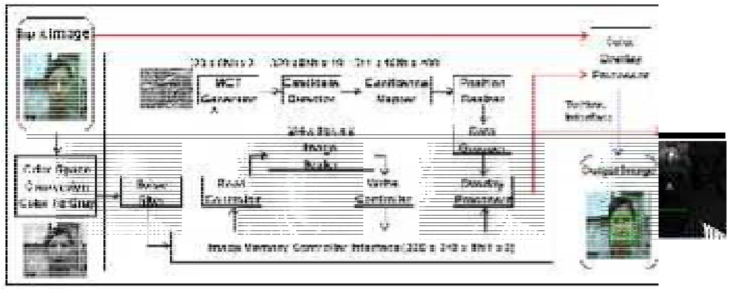


Figure 1: Block Diagram of Proposed Face-Detection Engine

IV. EXPERIMENTAL RESULT

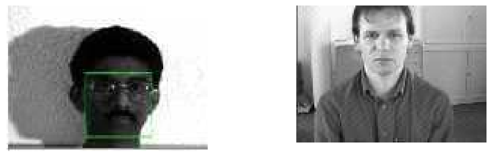
The developed face detection system has verified superb performance of 99.76 % detection-rate in various illumination environments using Yale face database [4] and BioID face database [5] as shown in Table 1, Table 2, and Figure 2. And also we had verified superb performance in real-time hardware though FPGA as shown in figure 3. The developed face- detection FPGA system can be processed at a maximum speed of 149 frames per second in real-time and detects at a maximum of 32 faces simultaneously. consequently, we verified developed face-detection engine at real-time by 30 frames per second within 13.5 MHz clock frequency with 226 mW power consumption.

Table 1: FPGA Test Results

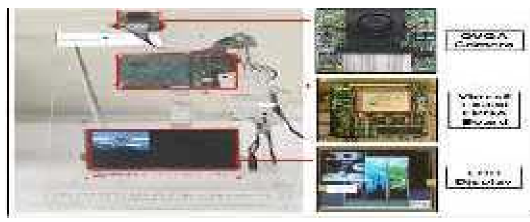
Test Results	The Amount Used
The Maximum Operating Frequency	54Mhz
The Maximum Processing Speed	149 Frame/sec
The Number of Simultaneous Face Detection	32 Face or more
Face Detection Ratio(Yale db and BioID db)	99.76 % (1682/1686)

Table 2: Face Detection Result (Yale Test Set And Bioid Test Set)

Type	Detection rate	False-positives rate
Yale Test set [6]	100 % (165/165)	0 % (0/165)
BioID Test set [7]	99.74 % (1517/1521)	0.20% (3/1521)
Average	99.76 % (1682/1686)	0.18 % (3/1686)



(a) Result in Various illumination Conditions,
(b) Results from Yale and BioID Face DB
Figure 2: Face Detection Results



(c) FPGA Development Environment
Figure 3: FPGA verification environment

V. CONCLUSION

This paper has verified a process that overcomes low detection rates caused by variations in illuminations thanks to the MCT techniques. The proposed face-detection hardware structure that can detect faces with high reliability in real-time was developed with optimized learning data through the Adaboost algorithm. Consequently, the developed face- detection engine has strength in various illumination conditions and has ability to detect 32 various sizes of faces simultaneously.

The developed FPGA module can detect faces with high reliability in real-time. This technology can be applied to human face-detection logic for cutting-edge digital cameras or recently developed smart phones. Finally, face-detection chip was developed after verifying and implementing through FPGA and it has advantage in real-time, low power consumption and low cost. so we can expect good efficiency with high resolution and detection rates for all required applications.

REFERENCE

1. Paul Viola and Michael J. Jones, “Robust real-time face detection” In International Journal of Computer Vision, pp. 137-154, 2004.
2. Yoav Freund and Robert E. Schapire. "A decision-theoretic generali- zation of on-line learning and an application to boosting" in Journal of Computer and System Sciences, pp. 119-139, 1997.
3. Bernhard Froba and Andreas Ernst, "Face detection with the Modified Census Transform", IEEE International Conference. On Automatic Face and Gesture Recognition, pp. 91-96, Seoul, Korea, May. 2004.
4. Georghiades, A. : Yale Face Database, Center for computational Vision and Control at Yale University, http: //cvc.yale.edu /projects /yalefaces/yalefa

5. The BioID face database: [http : //www.bioid.com /downloads /facedb /face data base .html.
6. Dongil Han, HyunjongCho, Jongho Choi, Jaeil Cho, "Design and Implementation of real-time high performance face detection engine",SP(Signal Processing), 47th Book, 3 Issue,The Institute of Electronics Engineersof Korea Publication(IEEK), March, 2010.
7. K.Venkararamani, S.Qidwai and B.VijayKumar, “Face Authentication from Cell Phone Camera Images with Illumination and Temporal Variations”, IEEE Transaction on System, Man and Cybernetics, 2005.