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A COLUMN-DECOUPLED 9T CELL FOR LOW POWER DIFFERENTIAL AND DOMINO-BASED SRAM DESIGN

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Abstract— Embedded memories are widely used in low power system on chip. Low power performance can optimized with process, circuit, architecture and system level co-development. Static random access memories consist of almost 90% of Very Large Scale Integration (VLSI). In this project, Low power design considerations are described in advanced technology nodes to address memory leakage and active power dissipation. Memory bit cell design in context of process technology definition; Circuit techniques at the macro design level and chip level integration consideration of low power are described. A novel half-select disturb transistor SRAM cell are introduced. This together with elimination of half select disturbs enhance the overall array by implementing the low power VLSI. The floating body effect is shown to degrade the read stability while improving the write stability. The Stability and speed of cell are deteriorated which can be improved by proper sizing of the tail transistor. A short bit line loading of 16 cell/ BL is adopted to achieve high-performance in read logic operation. The number of system accesses into the actual memory will be reduced by size of this" output cache". This made the system to achieve the high performance under read and write operation, Comparison was made between the 8T-CDC and default 6T cell. Cache memories are hits at high rate in 8T comparing to the 6T and elimination of half select with comparable access time as 6T-Based designs, The Vdd_{min} minimize due to switching circuit, Hence power consumption are achieve. The simulation results are show improvement of cell Vdd_{min} over traditional 6T and 8T cells for PD/SOI technology.

Keywords - *Column-Decoupled, Differential/Domino Read, Half-select, Low power, 8T, SRAM, Stability.*

I. INTRODUCTION

Low power VLSI is a broad concept that refers to the power consumption of a system design on a chip. The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bi-stable latching circuitry made of Transistors/MOSFETS to store each bit. Compared to Dynamic RAM (DRAM). SRAM doesn't have a capacitor to store the data, hence SRAM works

without refreshing. In SRAM the data is lost when the memory is not electrically powered. RAM is faster and more reliable than the more common DRAM. While DRAM supports access times (access time is the time required to read or write data to/from memory) of about 60 nanoseconds, SRAM can give access times as low as 10 nanoseconds. In addition, its cycle time is much shorter than that of DRAM because it does not need to pause between accesses. Unfortunately, it is also much more expensive to produce than DRAM. Due to its high cost, SRAM is often used only as a memory cache.

The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors [1]. When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile (i.e., the data is lost when the power is removed). However, the data does not "leak away" like in a DRAM, so the SRAM does not require a refresh cycle.

II. COLUMN SELECT (HALF-SELECT) AND MEMORY DESIGN

Half-selected cells are defined as the cells on the activated word-line whose bit lines are not activated (e.g. remain in the pre-charged state and not pulled low). The stability of these cells is reduced when compared to an uncased cell, both during read and write. An asymmetric 6T cell with similar sizing but a single WL has a worse half-select RSNM during both read and write.

However, with the dual word-line scheme, NR is turned off during a read and the half-select RSNM is the RSNM of the stronger side (e.g. P1-N1-NA). Thus we reduce the half-select issue during a read when compared to a single-WL asymmetric cell as well as a conventional 6T. As shown by the distributions, the mean RSNM for half-selected cells during read improves by 18% under nominal operating conditions [2]. The spread of the distribution increases, but the RSNM of the asymmetric 6T is always greater than that of the conventional.

We can get around the half-select problem by writing the entire row or by using a read-modify-write technique. Thus an alternative implementation of our proposed bit cell would involve using a single WL, while keeping the same device sizes, and use one of the above approaches to solve the half-select issue. Another solution would be to make NR weaker by using a higher VT device or by reducing its width. Since the half-cell P2-N2-NR is already sized for write, we need not make NR as wide as NA. While this would also reduce the cell area, we chose not to do this since it would reduce the gains in write margin for the write ‘1’ case and worsen the impact of variation.

III. 8T COLUMN DECOUPLED CELL

The cell is 6T based and utilizes decoupling logic. It employs gated inverter SRAM cells to decouple the column select read disturb scenario in half-selected columns which is one of the impediments to lowering cell voltage. Furthermore, “false read” before write operation,

common to conventional 6T designs due to bit-select and word line timing mismatch, is eliminated using this design.

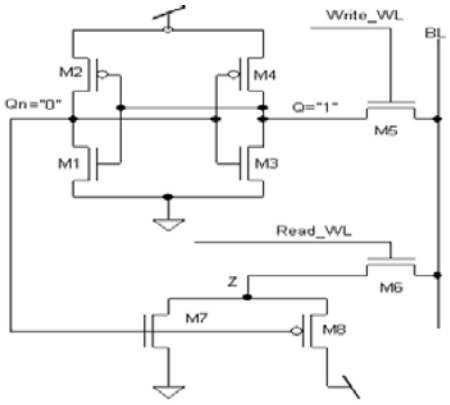

Figure 1: 8T SRAM Design

Two design styles are studied to account for the emerging needs of technology scaling as designs migrate from 90 to 65 nm PD/SOI technology nodes. For the sense Amp based design, read disturbs to the fully-selected cell can be further minimized by relying on a read-assist array architecture which enables discharging the bit-line (BL) capacitance to GND during a read operation. This together with the elimination of half-select disturbs enhance the overall array low voltage operability and hence reduce power consumption by 20%–30%. The domino read based SRAM design also exploits the proposed cell to enhance cell stability while reducing the overall power consumption more than 30% by relying on a dynamic dual supply technique in combination of cell design and peripheral circuitry[3]. Because half-selected columns/cells are inherently protected by the proposed scheme, the dynamic supply “High” voltage is only applied to read selected columns/cells, while dynamic supply “Low” is employed in all other situations, thereby reducing the overall design power. A short bit line loading of 16 cells/BL is adopted to achieve high-performance low-power operation and lower bit line capacitance to improve stability.

A newly developed fast Monte Carlo based statistical method is used to analyze such a unique cell, and 65 nm design simulations are carried out at 5 GHz. The feasibility of the cell and sensitivity to sense Amp timing has been proved by fabricating a 32 kb array in a 90-nm PD/SOI technology.

IV. DIFFERENTIAL AND DOMINO LOGIC

A. Differential Logic

Differential TTL is a type of binary electrical signaling based on the TTL (transistor-transistor logic) standard

Normal TTL signals are single-ended, which means that each signal consists of a voltage on one wire, referenced to a system ground. The "low" voltage level is zero to 0.8 volts, and the "high" voltage level is 2 volts to 5 volts. A differential TTL signal consists of two such

wires, also referenced to a system ground. The logic level on one wire is always the complement of the other. The principle is similar to that of low-voltage differential signaling (LVDS), but with different voltage levels, and even more similar to the RS-422 standard. Differential TTL is used in preference to single-ended TTL for long-distance signaling. In a long cable, stray electromagnetic fields in the environment, or stray currents in the system ground, can induce unwanted voltages that cause errors at the receiver. With a differential pair of wires, roughly the same unwanted voltage is induced in each wire. The receiver subtracts the voltages on the two wires, so that the unwanted voltage disappears, and only the voltage created by the driver remains.

A second advantage of differential TTL, when correctly terminated, is that the differential pair of wires forms a current loop. The driver sources a current from the power supply into one wire. This current passes along the wire to the receiver, through the termination resistor and back up the other wire, then back through the driver and down to ground. This arrangement prevents the signal from injecting currents into the ground connection, which might upset other circuits attached to it. Differential TTL is the most common type of high-voltage differential signaling (HVDS).

A. Domino Logic

Domino logic is a CMOS-based evolution of the dynamic logic techniques which were based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. It was developed to speed up circuits. In dynamic logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error. . One solution is domino logic, which inserts an ordinary static inverter between stages. While this might seem to defeat the point of dynamic logic, since the inverter has a PFET (one of the main goals of dynamic logic is to avoid PFETS where possible it works well [4].

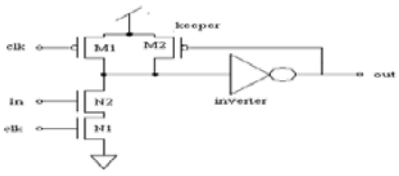

Figure 2: (a) Standard Domino Logic

First, there is no fan-out to multiple PFETS. The dynamic gate connects to exactly one inverter, so the gate is still very fast. And since the inverter connects to only NFETS in dynamic logic gates, it too is very fast. Second, the PFET in an inverter can be made smaller than in some types of logic gates[5]. In a domino logic cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clock cycle) just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic. The fig 2. (a) illustrates the standard domino based logic. It contrasts with other solutions to the cascade problem in which cascading is interrupted by clocks or other means.

V. SIMULATION ENVIRONMENT AND METHODOLOGY

In this section we compare and analyze the 8T CDC cell and traditional 6T thin cell with dynamic dual supply.

A. Dual-VDD Scheme

To improve the operating margins at low voltage, in this subsection, we apply the dual-Vdd scheme to both the 6T and 8T cells. Two fixed voltages (Va and Vmax, Vmax >Va) are provided to the SRAM cells, and the supply voltage in the memory cells (Vmc) and the word line (WL) voltage (Vwl) are switched according to the read and write conditions. In this paper, Vmax is set to 1.0V as a nominal voltage. In a read operation, Vmc is set to Vmax that stabilizes a stored datum, which maximizes a read margin. Alternatively in a write cycle, Vwl is set to Vmax as illustrated in Fig. 2. (b) which increases the conductance of the access transistors. This operation makes a bitline datum easily written, and thus improves the write margin. On the other hand, in the 8T cell, the write-WL (WWL) voltage (Vwwl) is merely set to Vmax as shown in Fig. 2.(b), since we do not have to pay attention to the read margin[6].

A. Improvement of Operating Margins

The improvement of the operating margins with the dual- Vdd scheme, where a global Vth variation of the triple standard deviation is reflected. As for the random Vth variation, 6σvth is considered in an SRAM cell. In the milky-way plots, the read margin cannot be obtained on the left side from the read limit curve, where a stored datum possibly flips in read operation. Similarly, the write margin is not satisfied on the right side from the write limit curve. In the 6T-cell case, the read and write, Margins are both obtained in the region between the read and write limit curves, which means that the 6T cell works logical Vth of the cell inverter higher and helps stable “H”-write operation at the “L”-stored node.

B. Comparison of8T and 6T SRAM

The present invention is directed to an 8TSRAM Architecture, The Memory operation like fetching and storing are get improved by DVS(Dual Voltage Scheme).This are Explained in similar aspect given below. SRAM is speed, Here the usage of the DVS are getting the SRAM in improvement in read and write operation hence speed is increase is optimized. Considering a 0.7-V operation at the 32-nm node, the area of the 6T cell is smaller by 64.4% in the dual-Vdd scheme than the single-Vdd scheme.

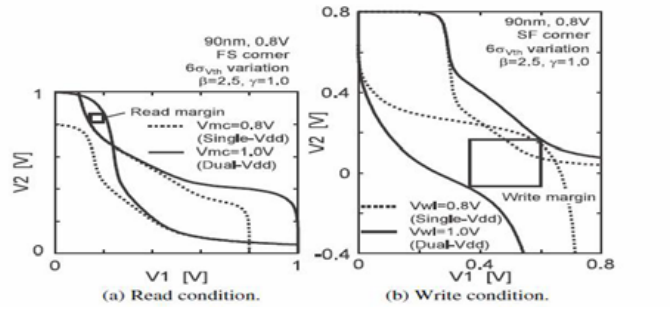

Figure 2: (b) Read and write condition

A second aspect of present invention is to provide the Area comparisons of SRAM8T with 6T Architecture, The transistor length (L) of each transistor is set to the minimum (Lmin = design rule).The load transistor has the minimum channel width (Wmin). Lmin and Wmin are scaled by 0.7 time per generation. In the 6T cell, the channel width of the access transistor (WA) is first optimized for the write margin, on the condition of Wd = Wmin (Wd: the channel width of the drive transistor). Then, WD is optimized for the read margin. In the 8T cell, we merely optimize WA for the write margin. WD is set to Wmin since the read margin can be neglected. A third aspect of present invention is to provided the power consumption, here due to the presence of dual Vdd scheme the biasing voltage are get divided at beginning and switching of voltage are done in active (on) and de-active (off) region, Hence power consumption can achieve. Due to the Dual Vdd the 40% of power consumption can achieve comparing to the 6T SRAM architecture. A fourth aspect of present invention there are improvement in cache memory, This is done by mean of adding the extra logical transistor construction under the domino and differential logic design, Hence compared with the 6T SRAM architecture the cache memory are hit over 55% in 8TSRAM design. The following shows that the theory followed to achieve those aspect in construction of 8TSRAM column decoupled transistor logic.

C. Floating-Body Dynamic Supply Boosting Technique

The proposed scheme requires only single supply and exploits the capacitive coupling effects between the gate, body, and source of a floating-body PD/SOI device. Depending on the bias conditions and signal transition, the gate-to-body and body-to-source couplings can be quite strong. We exploit this capacitive coupling characteristics first time to dynamically boost the virtual array supply voltage. The boost can be either column-based or row-based. The boost transistor consists of a floating-body PD/SOI NFET with its gate controlled by “cklbswc” signal. In standby, “cklbswc” is “Low”, thus the virtual array supply voltage “Vdd v” is at “Vdd ”. With both its drain and source at “Vdd”, the floating-body of the booster NFET is at “Vdd” as well. During Read operation, the “cklbswc” signal ramps to “High”, thus turning off the PFET header.

The ramping up of the gate signal “cklbswc” is capacitive coupled to the floating-body of the booster NFET, thusbringing the floating-body potential to a level significantly above Vdd. As such, the source node of the booster NFET (which is the virtual array supply node) is capacitive coupled up by the body to source capacitance. Notice that: although there is some coupling from the gate directly to the source, through the gate-to source overlap capacitance, the gate-to-source overlap capacitance and coupling is significantly smaller than the gate-to-body coupling; as both its drain and source are at “Vdd ”, the booster NFET never turns “On”. As such, the inversion channel never forms, and the body is never shielded from the gate. Thus, the gate-to-body coupling occurs (is effective) through the entire gate signal ramping; and the capacitive coupling effect is “instantaneous” (on the order of the dielectric relaxation time of the materials), thus the body and source voltage “follow” the gate ramping almost immediately.

VI. DOMINO BASED APPORACH ANALYSIS AND RESULTS

The Implementation of the Domino based logic using tanner is given below the following Fig 3. (a) And 3(b), show that the 8T SRAM design and its corresponding output in S-Edit and W-edit respectively.

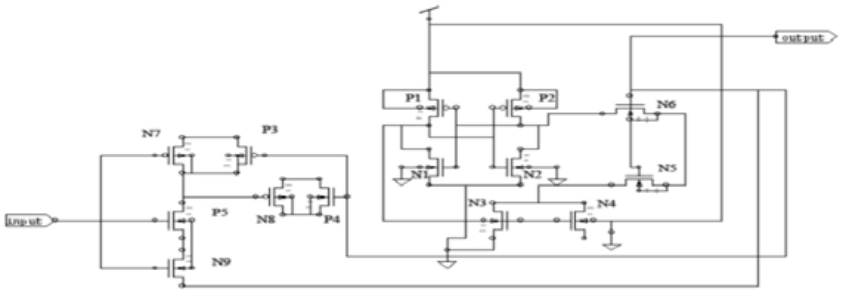

Figure 3: (a) Schematic diagram for 8T with Domino Logic

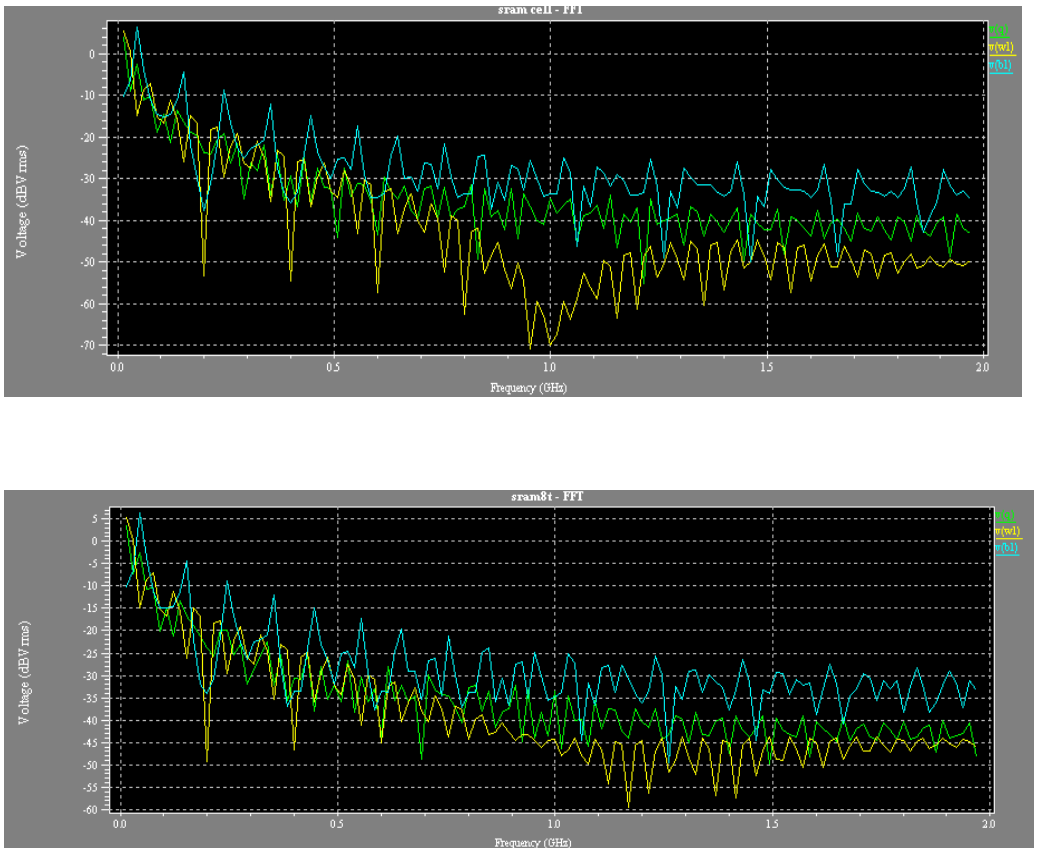

Figure 3: (b) Hardware-based access time screen shots for 6T and 8T-CDC cell indicate negligible difference.

W-Edit of 6T SRAM Design are consist of mismatching of read and write synchronization that has been rectified by mean of replacing 8T SRAM the read and write future synchronized.

VII. CONCLUSION

In this paper, we clarified that, in the dual-Vdd scheme, the area of the 6T SRAM cell keeps the area smaller than that of the 8T SRAM cell, over feature process nodes. In contrast, in the DVS scheme, the 8T cell is preferable in a 32-nm process technology. The DVS scheme saves the 8T cell area by 4.9% compared with the 6T-cell case in the 32-nm node. Considering a 0.7-V operation at the 32-nm node, the area of the 6T cell is smaller by 64.4% in the dual-Vdd scheme than the single-Vdd scheme. The DVS scheme achieves the area saving of 55.2% with the 8T cell, compared with the 6T cell in the single-Vdd scheme, Cache Memory are Hits at 55% comparing to the 6T SRAM Architecture.

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