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# Switching Activity Reduction Using Scan Shift Operation

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**Abstract-**This paper presents BIST TPG (built in self test) for low power dissipation and high fault coverage a low hardware overhead test pattern generator (TPG) for scan-based built-in self-test (BIST) that can reduce switching activity in circuits under test (CUTs) during BIST and also achieve very high fault coverage with reasonable lengths of test sequences. The proposed BIST TPG subside transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. The proposed BIST is comprised of two TPGs: LT-RTPG and 3-weight WRBIST. Test patterns engender by the LT-RTPG detect easy-to-detect faults and test patterns generated by the 3-weight WRBIST detect faults that abide undetected after LT-RTPG patterns are applied. The proposed BIST TPG does not require modification of delegation logics, which can lead to performance degeneracy. The 3-weight weighted random BIST techniques to reduce test sequence lengths by improving detection probabilities of random pattern resistant faults. A forthright solution is to reduce the speed of the test clock during scan shift operations. However, since most test application time of scan-based BIST is expend for scan shift operations, this will increase test application time by about a factor of if scan flip-flops are clocked at speed during scan shift operations. The proposed BIST can suggestive reduce switching activity during BIST while achieving 100% fault coverage .Larger reduction in switching activity is achieved in large circuits.

**Keywords:** *Built-in-self-test (BIST), Test pattern generator (TPG), LT-RTPG (Low transition random test pattern generator), 3WR-BIST (3 Weight Random Test Pattern Generator),Switching activity, heat dissipation during test application, low power testing, power dissipation during test application, random pattern testing.*

## I. INTRODUCTION

Technology provides smaller, faster, and lower energy devices which allow more powerful and compact circuitry. However, these benefits come with a cost—the Nano Scale devices may be less reliable. Thermal- and shot-noise estimations alone suggest that the fault rate of an individual Nano Scale device may be orders of magnitude higher than today's devices. As a result, we can expect combinational logic to be susceptible to faults. So, in order to test any circuit or device we require separate testing technique which should be done automatically. For that purpose, we are going for BIST (Built In Self Test).

The Built-In Self-Test (BIST) [1], test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware, minimizing hardware overhead is a major concern of BIST implementation. Unlike stored pattern BIST, which requires high hardware overhead due to memory devices required to store precompiled test patterns, pseudorandom BIST, where test patterns are generated by pseudorandom pattern generators such as linear feedback shift registers (LFSRs), requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR often require unacceptably long test sequences thereby resulting in prohibitively long test time. The random pattern test length required to achieve high fault coverage is often determined by only a few RPRFs.

In this project, I propose a low hardware overhead scan based BIST technique that can achieve very high fault coverage without the risk of damaging CUTs due to excessive switching activity during BIST. Recently, techniques to reduce switching activity during BIST have been proposed in [7] and [2]–[5].A straightforward solution is to reduce the speed of the test clock during scan shift operations.

A BIST TPG that can achieve high fault coverage and also reduce switching activity during BIST is proposed for single scan chain designs in, which augments the LT-RTPG with the serial fixing 3-weight WRBIST. It is shown that the 3-weight WRBIST can achieve very high fault coverage with low hardware overhead. The LTRTPG proposed in generates correlated test patterns that can reduce transitions at state inputs during scan shift operations. The serial fixing 3-weight WRBIST can also generate test patterns that cause less switching activity during BIST

In weighted random pattern testing [4], the outputs of test pattern generator (TPG) are biased to generate test sequences that have non-uniform signal probabilities to increase detection probabilities of RPRFs that escape pseudorandom test sequences, which have a uniform signal probability of 0.5. Random pattern generators proposed in [6] and [3] use Markov sources to exploit spatial correlation between state inputs that are consecutively located in the scan chain.

A 3-weight weighted random BIST (3-weight WRBIST) can be classified as an extreme case of conventional weighted random pattern testing BIST. However, in contrast to conventional weighted random pattern testing BIST where various weights, e.g., 0, 0.25, 0.5, 0.75, 1.0, can be assigned to outputs of TPGs, in 3-weight WRBIST, only three weights,0, 0.5, and 1, are assigned. Since only three weights are used, circuit to generate weights is simple; weight 1 (0) is obtained by fixing a signal to a 1 (0) and weight 0.5 by driving a signal by an output of a pseudorandom pattern generator, such as an LFSR.

The remainder of the paper is organized as follows: Section II presents the exiting method for fault Diagnosis. Section III discusses the description of. Architecture of BIST and proposed block diagram of BIST TPG. Section IV describes the minimizing switching activity during BIST (LT-RTPG, 3-Weight WRBIST). Section V presents the Simulation results and Section VI concludes the paper with the future prospects.

## II. FAULT DIAGNOSIS

LFSR is mainly used to generate patterns. Scan chain is a group of registers. Here the scan chain is mainly used to store the patterns generated from LFSR. These patterns are applied to CUT and the outputs generated from CUT are again stored in scan chain. For every input response stored in scan chain the corresponding output patterns are stored in the scan chain i.e., located at the output of the CUT. Here in comparator, it compares the input to CUT and corresponding output of CUT. And here if there is a difference obtained at the output of the comparator fault will be detected, else there is no fault in the circuit. Here more hardware overhead is implemented, Due to this structure more number of transitions occurred and hence more power is consumed. In order to reduce the power consumption with high efficiency we need to include extra circuitry.

Figure 2.1.Existing method for fault diagnosis. There are three types of faults that often occur:
1) Soft errors
2) Hard errors
3) Unhandled errors

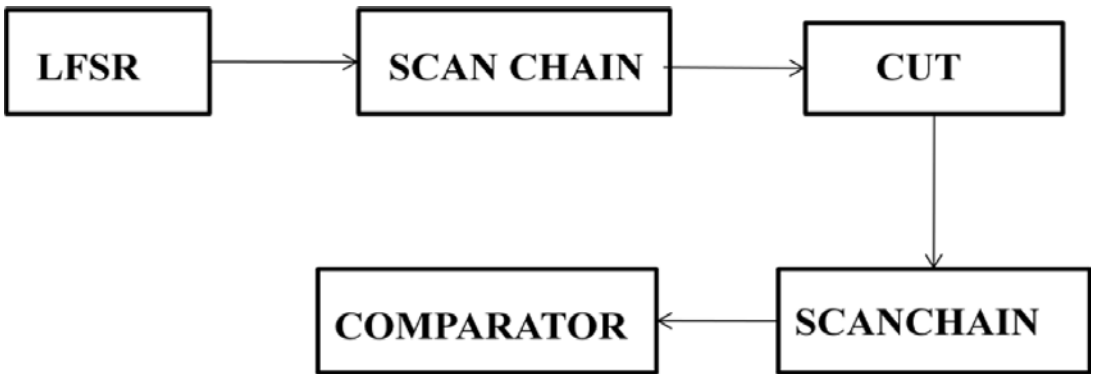


Figure 2.1: Exiting Method for Fault Diagnosis

### 2.1.1 Soft errors

Soft errors usually happen due to handling mistakes. Coppermine will display an error message, but we can continue to browse the gallery. The soft errors are fully localized so the programmers of Coppermine have (more or less) anticipated that such an error may happen under certain circumstances.

### 2.1.2 Hard errors

Hard errors are messages that won't go away, usually because something is broken and needs fixing. This is usually the case if something is wrong with the database. As a result, you will see the reared "Fatal error" message that usually doesn't mean much too inexperienced users. Hard errors usually indicate that something is wrong which the programmers of Copper mine could not foresee, that's why only a generic error message is being displayed.

### 2.1.3 Unhandled errors

Unhandled errors are the ones that usually are most tricky to solve, as they make the application Coppermine crash in mid-air, without a meaning full error message that could tell users what is wrong. This is usually the case if you get a blank page or just a template error.

**Fatal Error**

The message "Fatal Error" is a generic error message that just says that there is something wrong. It usually is a hard error we won't be able to continue using Copper mine unless we fix the reason for the error message. The reasons for such a generic error message are manifold. For security reasons the "real" error message is not being displayed by default, but only the generic "Fatal Error" message.

**Stuck-at faults**

Types of stuck-at-faults are
1) Single stuck-at-faults
2) Multiple stuck-at-faults
Three properties define a single stuck-at
1) Fault only one line is faulty
2) The faulty line is permanently set to 0 or 1
3) The fault can be at an input or output of a gate

## III. BUILT-IN SELF TEST (BIST)

Built-in Self Test(BIST) is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

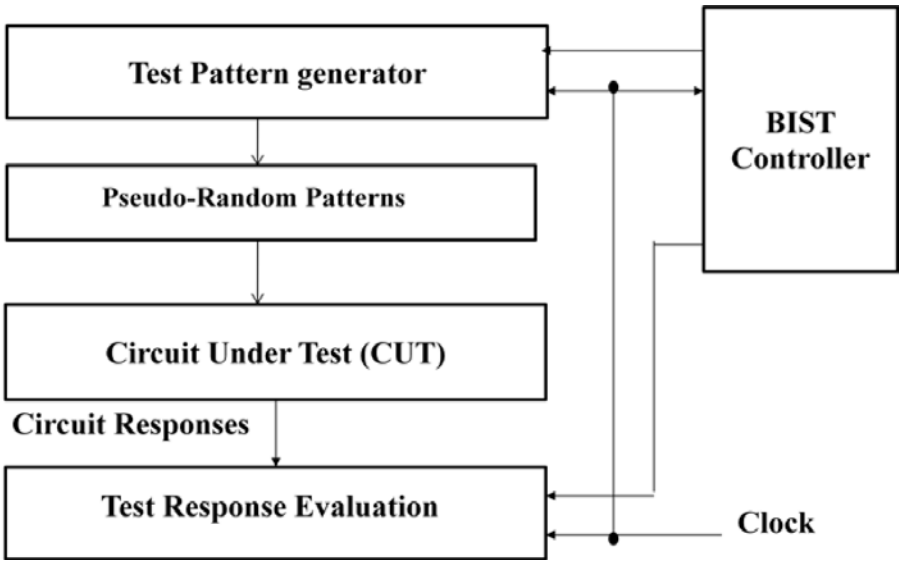


Figure 3.1: Architecture of BIST

In built-in self-test (BIST) (Fig 3.1), internal hardware is used to generate test patterns that are applied to the circuit-under-test and to analyze the output response. BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. Built-in self-test (BIST), test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware, minimizing hardware overhead is a major concern of BIST implementation. Unlike stored pattern BIST, which requires high hardware overhead due to memory devices, required to store.

Where test patterns are generated by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR often requires unacceptably long test sequences thereby resulting in prohibitively long test time.

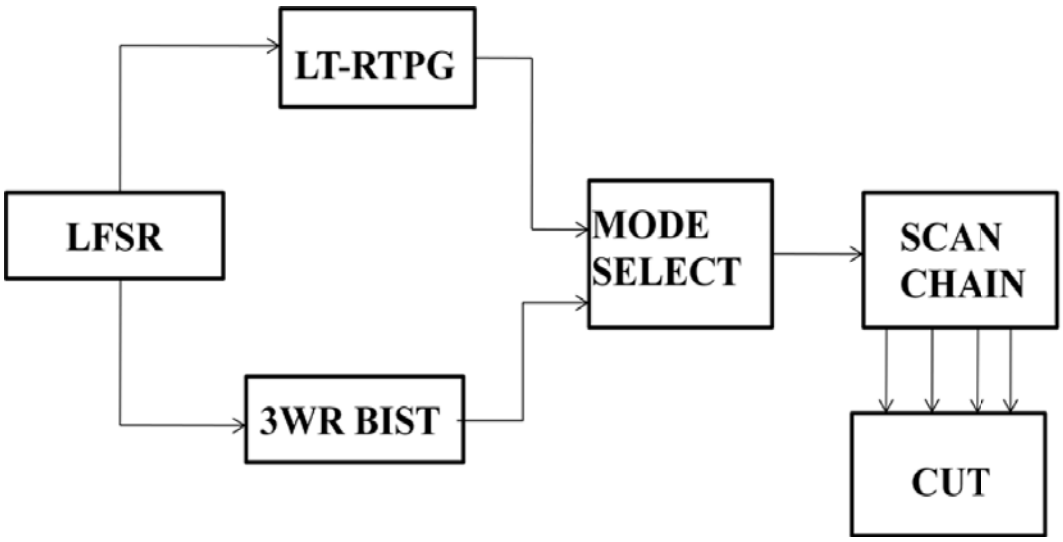


Figure 3.2: Proposed Block Diagram of BIST TPG

The random pattern test length required to achieve high fault coverage is often determined by only a few RPRFs.

Figure 3.2 Block diagram of BIST TPG Here the patterns generated from LFSR is given to LT-RTPG and 3 Weight WRBIST .Mode select is mainly used to select the faults detected from LT-RTPG or from 3Weight WR-BIST i.e. the undetected faults from LT-RTPG. And is given to scan chain for shifting and storing of patterns and then to CUT. As more switching activities causes damage to the circuit. Here the LT-RTPG reduces switching activities in the circuit so that the number of transitions will be reduced and less power will be consume.

## IV. LINEAR FEEBACK SHIFT REGISTER

An alternative approach for generating a pseudo exhaustive test set is to use a combination of an LFSR and an SR. In an LFSR, the outputs of a selected number of stages are fed back

to the input of the LFSR through an EX-OR network. An n-bit LFSR can be represented by an irreducible and primitive polynomial. If the polynomial is of degree n, then the LFSR will generate all possible 2n−1 nonzero binary patterns in sequence; this sequence is termed the maximal length sequence of the LFSR.

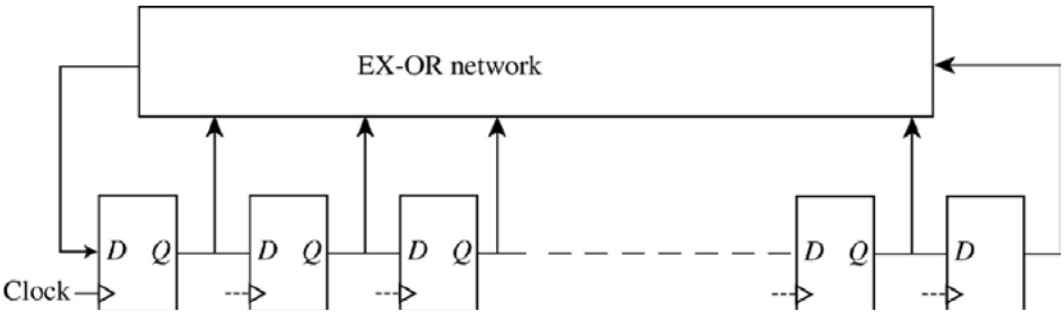


Figure 3.3: General Representation of an LFSR**.**

**Minimizing Switching Activity During BIST**

The BIST TPG proposed in this paper reduces switching activity in the CUT during BIST by reducing the number of transitions at scan inputs during scan shift cycles. If scan input pi is assigned v, where v(0,1), at a time t-1 and assigned v' at time t, then transition occurs at pi at time t. the transition that occurs at scan input pi can propagate into internal circuit lines causing more transitions. During scan shift cycles, the response to the previous scan test pattern is also scanned out of the scan chain. Hence, transitions at scan inputs can be caused by both test patterns and responses.

Since it is very difficult to generate test patterns by a random pattern generator that cause minimal number of transitions while they are scanned into the scan chain and whose responses also cause minimal number of transitions while they are scanned out of the scan chain, we focus on minimizing the number of transitions caused only by test patterns that are scanned in. Even though we focus on minimizing the number of transitions caused only by test patterns, our extensive experiments show that the proposed TPG can still reduce switching activity significantly during BIST .Since circuit responses typically have higher correlation among neighborhood scan outputs than test patterns, responses cause
Fewer transitions than test patterns while being scanned out.

**A. LT-RTPG (LOW TRANSITION-RANDOM TEST PATTERN GENERATOR)**

This is a low hardware overhead test pattern generator (TPG) for scan-based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence. Since the correlation between consecutive vectors applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation. Excessive switching activity during test application can damage CUTs during BIST.

The LT-RTPG (Figure 4.1) reduces switching activity during BIST by reducing transitions at scan inputs

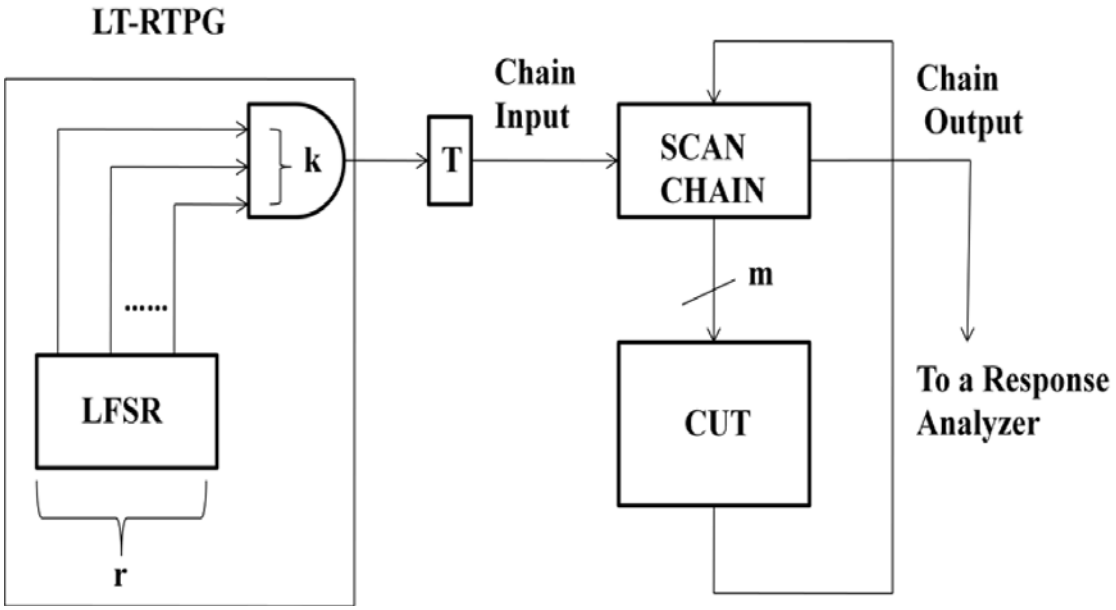


Figure 4.1: Architecture of LT-RTPG

During scan shift operations. The LT-RTPG is comprised of an r-stage LFSR, a K-input AND gate, and a toggle flip-flop (T flip- flop). Hence, it can be implemented with very little hardware. Each of K inputs of the AND gate is connected to either a normal or an inverting output of the r LFSR stages. If large k is used, large sets of neighboring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in Test sequence length. LT-RTPGs with K=2 or 3 are used. Since a T flip-flop holds previous values until the input of the T flip-flop is assigned a 1, the same value v, where v {0,1} is repeatedly scanned into the scan chain until the value at the output of the AND gate becomes 1.

Hence, adjacent scan flip-flops are assigned identical Values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations, thus the LT-RTPG can reduce Heat dissipation during overall scan testing. It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from apparent test vectors.

This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits. The LT-RTPG can attain high fault coverage without excessive switching activity or large area overhead even for circuits that have large numbers of RPRFs.

## B. WEIGHT WRBIST (3-WEIGHT WEIGHTED RANDOM BIST)

If a large set of scan inputs that are consecutively located in the scan chain are assigned identical values (X is identical to any binary value 0 or 1) in a generator, then the flip-

flops$TF_0$ and $TF_1$ of 3-Weight WRBIST (see Figure 4.2) stay at the same state for many scan shift cycles. While $TF_1$ holds a 1, the output of the OR gate in the fixing logic is set to a 1 and 1's are continuously scanned into the scan chain and no transitions occur at the input of the scan chain.

Likewise, $TF_0$ while holds a 1, random pattern values generated by the LFSR are blocked at the AND gate and no transition occurs at the input of scan chain provided that the other T flip-flop $TF_1$ does not toggle. Hence, in order to significantly reduce the number of transitions at the input of scan chain, either $TF_0$ or $TF_1$ should be assigned a 1 and stays at the 1 for long periods of scan shift cycles.

Figure 4.2 shows an implementation of the 3-weight WRBIST for the generators shown in Figure 4.2 The shift counter is an (m+1) modulo counter, where m is the number of scan elements in the scan chain (since the generators are 9 bits wide, the shift counter has 4 stages). When the content of the shift counter is k, where k=0, 1….8, a value for input $p_k$ is scanned into the input of scan chain. The generator counter selects appropriate generators; when the content of the generator counter is i test patterns are generated by using gen(C(i)), where i=0,1,2

Pseudo-random pattern sequences generated by an LFSR and a CA are modified (fixed) by controlling the AND and OR gates with overriding signal $s_0$ and $s_1$, fixing a random value to a 0 is achieved by setting $s_0$ to a 1 and to a 0 and fixing a random value s1 to a 1 is achieved by setting to a1 (since a random value can be fixed $s_1$ to a 1 by setting to a 1 independent of the state of s0 , the state of s0 is a don't care). Overriding signals s0 and $s_1$ are driven by the outputs of T flip-flops, and. The inputs of FLIP FLOPS and are in turn driven by the outputs of the decoding logic D0 and D1 respectively, which are generated by the outputs of the shift counter and the generator

The shift counter is required by all scan-based BIST techniques and not particular to the proposed 3-weight WRBIST scheme. All BIST controllers need a pattern counter that counts the number of test patterns applied. The generator counter can be implemented from(log g) MSB (most significant bit) stages of the existing pattern counter, where g is the number of generators, and no additional hardware is required for the generator counter.

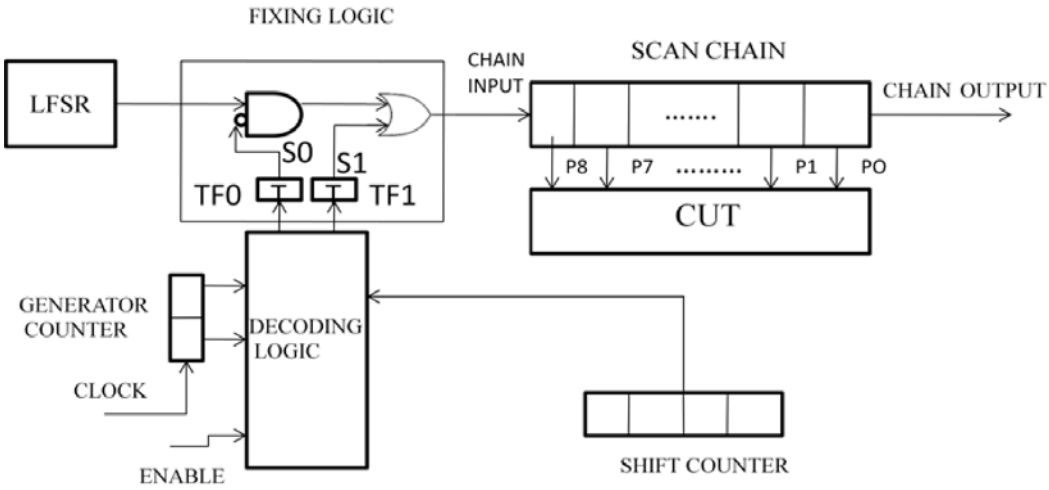


Figure4.2: Architecture of 3-Weight WRBIST

Hence, hardware overhead for implementing a 3-weight WRBIST is incurred only by the decoding logic and the fixing logic, which includes two toggle flip-flops (flip-flops), an AND and an OR gate. Since the fixing logic can be implemented with very little hardware, overall hardware overhead for implementing the serial fixing 3-weight WRBIST is determined by hardware overhead for the decoding logic.

## V. SIMULATION RESULT

**Linear Feedback Shift Register**

LFSR O/P is shown in figure 5.1. The wave form shows that if inputs are high, clock, clock input and reset high as assigned for operation then the output is 00000000.

From I can conclude that Pseudo-random pattern sequences generated by an LFSR

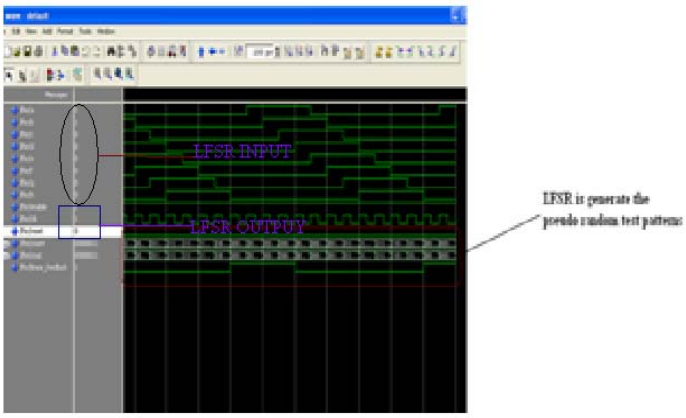


Figure 5.1: Linear Feedback Shift Registers

**Title**: LFSR

Table 5.1.1 LFSR Output Description

| Input | | | Output | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock | Enable | Reset | a | b | c | d | e | f | g | h | Input of LFSR is enable=1, reset=0 than LFSR produce the out of sequence is 11000000 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Low Transition Random Test Pattern (LT-RTPG)**

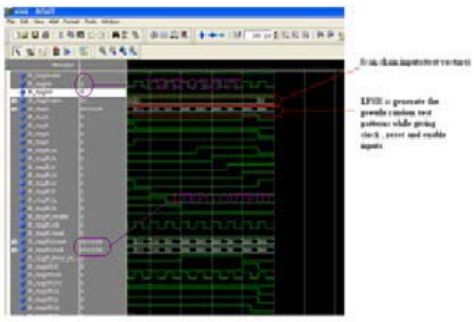

Figure 5.2 Low Transition Random Test Pattern (LT-RTPG)

Here an endeavor has been made to analyze the performance of LT-RTPG from that we can conclude that if inputs are high, clock, clock input and reset high as assigned for operation then the LFSR output is 00000000 and Scan chain output is 00.

From I can conclude that scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations, thus the LT-RTPG can reduce Heat dissipation during overall scan testing

## VI. CONCLUSION & FUTURE PROSPECTS

This paper presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with an arguable length of test sequence. The test patterns are engender by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR often require unforeseeable long test sequences thereby resulting in prohibitively long test time. The proposed TPG LT-RTPG and 3-weight WRBIST reduces switching activities in the circuits, so that the number of transitions will be debase and less power will be consume.

**Future Prospects**

Instant of LFSR we use dual speed LFSR .It will generate pseudo random test patterns. It runs faster as compared to LFSR.

## VII. ACKNOWLEDGEMENT

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