Journal of Computer Applications ISSN: 0974 – 1925,
Volume-5, Issue EICA2012-3, February 10, 2012

A Survey on Sequential Elements for Low Power Clocking System

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Abstract— Low power flip-flops which plays a vital role for the design of low-power digital systems. Flip flops and latches consume a large amount of power due to redundant transitions and clocking system. In addition, the energy consumed by low skew clock distribution network is steadily increasing and becoming a larger fraction of the chip power. Almost, 30% - 60% of total power dissipation in a system is due to flip flops and clock distribution network. In order to achieve a design that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops and latches. We survey a set of flip flops designed for low power and High performance.

Keywords— *Flip flop; Low power; CMOS Circuit.*

I. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. One of the important factors is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the power consumption of the flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance.
Power Consumption is determined by several factors including frequency f, supply voltage, data activity, capacitance, leakage and short circuit current.

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

In the above equation, $P_{dynamic}$ is called the switching power $p=\alpha Cv^2f$. $P_{shortcircuit}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period $P_{short\ circuit} = I_{short\ circuit} * Vdd$. $P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the subthreshold leakage current. $P_{leakage\ current} = I_{leakage\ current} * Vdd$.

Based on the above factors, there are various techniques for lowering the power consumption shown as follows: In Double Edge Triggering [1],[2], Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. Double clock edge triggering method reduces the power by decreasing frequency. Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. The low swing method reduces the power consumption by decreasing voltage [3].

There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional capture flip-flop (CCFF)[8]) or clock gating, conditional discharge flip-flop (CDFF)[12]. In Conditional Operation, there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to avoid the redundant switching. In Clock Gating, when a certain block is idle, we can disable the clock signal to that block to save power. Both conditional operation and clock gating methods reduce power by decreasing switching activity[4].

In Reducing Short Current Power, split path can reduce the short current power, since p-MOS and n-MOS are driven by separate signals. In Reducing Capacity of Clock Load, 80% of non clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor[8]-[11],[13]. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity.

II. FLIPFLOP COMPARISON METRICS

There are several basic performance metrics that are used to qualify a flip-flop and compare it to other designs.

A. Clock-to-Q delay

Propagation delay from the clock input to the output Q terminal. This is assuming that the data input D is set early enough with respect to the effective edge of the clock input signal.

B. Setup time

The minimum time needed between the D input signal change and the triggering clock signal edge on the clock input. This metric guarantees that the output will follow the input in worst case conditions of process, voltage and temperature (PVT). This assumes that the clock triggering edge and pulse have enough time to capture the data input change.

C. Hold time

The minimum time needed for the D input to stay stable after the occurrence of the triggering edge of the clock signal. This metric guarantees that the output Q stays stable after the triggering edge of the clock signal occurs, under worst PVT conditions. This metric assumes that the D input change happened at least after a minimum delay from the previous D input change.

D. Data-to-Q delay

The sum of setup of data to the D input of flip-flop and the Clock-to-Q delay as defined above. Knowing that flip-flops are always in the critical path of a synchronous design standard cell library developers always try their best to minimize the setup time requirement of flip-flops and the Clock-to-Q delay to target the highest possible frequency for the design at hand. Hold times are not as critical as setup times and they do not impose an upper bound on the speed of a circuit in flip-flop based designs. On the other hand they are very critical in latch-based designs.

1. Stable region

Where the setup and hold times of a flip-flop are met and the Clock-to-Q delay is not dependent on the D-to-Clock delay. This is the required region of operation.

2. Metastable region

As D-to-Clock delay decreases, at a certain point the Clock-to-Q delay starts to rise exponentially and ends in failure. In this region, the Clock-to-Q delay is nondeterministic causing intermittent failures and behaviors which are very difficult to debug in real circuits not to mention silicon.

3. Failure region

Where changes in data are unable to be transferred to the output of the flip-flop. The optimal setup time noted on the graph would be the highest performance D-to-Clock delay to accomplish fastest D-to-output delay. Due to the steep curve to the left of that point not all library developers would target this value. Fig.1. shows an optimal setup time for D-to-Clock.

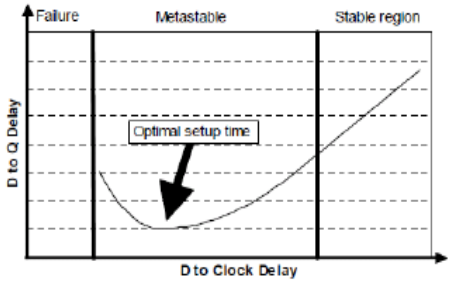

Figure 1: D-to-Clock

III. SURVEYED TECHNIQUES FOR REDUCING SWITCHING ACTIVITY

Most of the flip-flops presented here are dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose [8]–[13]. A brief survey of such techniques is conducted in this work, and the main techniques were classified as follows:

A. Conditional Capture Flip Flop

Conditional Capture technique is proposed for disabling redundant internal transitions [8] as shown in fig 2. This technique achieves significant power reduction at little or no delay penalties. Motivation behind Conditional Capture technique is the observation that considerable portion of power is consumed for driving internal nodes even when the value of the output is not changed (corresponding to low input activities). It is possible to disable internal transitions when it is detected that they will have no effect on output. But the drawback is increased set-up time for sampling zero (low level) and also heavier load is presented to the Q output of the flip flop.

B. Conditional Precharge Flip Flop

For overcoming the disadvantage in Conditional Capture Flip Flop, Conditional pre-charge flip flop is proposed [9][11] as shown in fig 3. One of the most important contributions of this work is related to preventing unconditional pre-charge operation of the internal node, tightly connected to excessive power dissipation of the circuit. This is accomplished by controlling the return of internal node to inactive (high) state, allowing the internal node to stay at low level until input condition is changed. This approach efficiently eliminates the unnecessary transitions of the internal node as well as race condition at the output. There are two main disadvantages: One is introducing another critical path for low input level capture. Another drawback is increasing the output load due to the feedback, which although minimal size transistor can be used, being out of the critical path, can affect total propagation delay.

C. Conditional Discharge Flip Flop

Conditional Discharge Flip-flop (CDFF) [12] not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small Q-to-output delay characteristics as shown in fig 4. With a data-switching activity of 37.5%, this flip-flop can save up to 39% of the energy with the same speed. In this Flip-flop, the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH. In this scheme, an n-MOS Transistor is inserted in the discharge path with the high-switching activity.When the input undergoes a LOW-to-HIGH transition, the output changes from HIGH to LOW. This transition at the output switches off

the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable. But the disadvantage is it used 15 clocked transistors.

D. Conditional Data Mapping Flip Flop

Conditional Data Mapping Flip flop used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors [13], hence CDMFF used less power than CCFF and CDFF as shown in fig 5. Note that CDFF used double edge clocking. For simplicity purposes, we did not include the power savings by double edge triggering on the clock distribution network. This shows the effectiveness of reducing clocked transistor numbers to achieve low power, Since CDMFF outperforms CCFF and CDFF. But it makes very difficult to apply the Double edge triggering and also it cannot be used in a low swing environment. Moreover it reduces the number of clocked transistors but it has redundant clocking as well as floating node. So we can move into the clocked pair shared flip-flop.

E. Clocked Pair Shared Flip Flop

Clocked Pair Shared flip-flop (CPSFF)[14] to use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF as shown in fig 6. In the clocked-pair-shared flip-flop, clocked pair is shared by first and second stage. An always on p-MOS, P1, is used to charge the internal node rather than using the two clocked pre charging transistors (P1, P2) in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors.

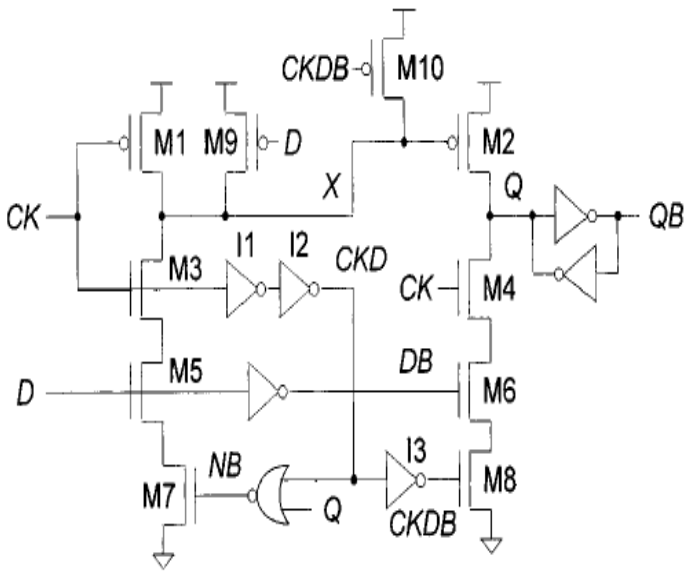

Figure 2: Conditional Capture Flip Flop

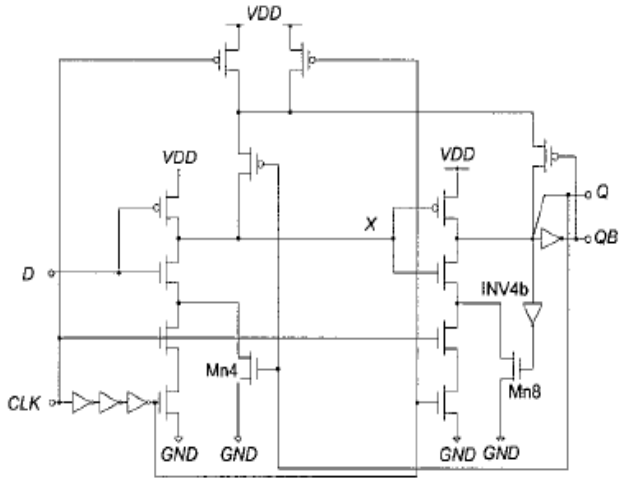

Figure 3: Conditional Precharge Flip-Flop

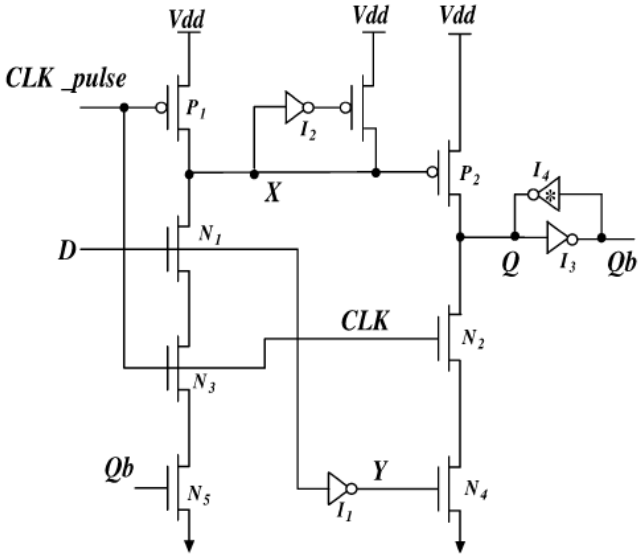

Figure 4: Conditional Discharge Flip Flop

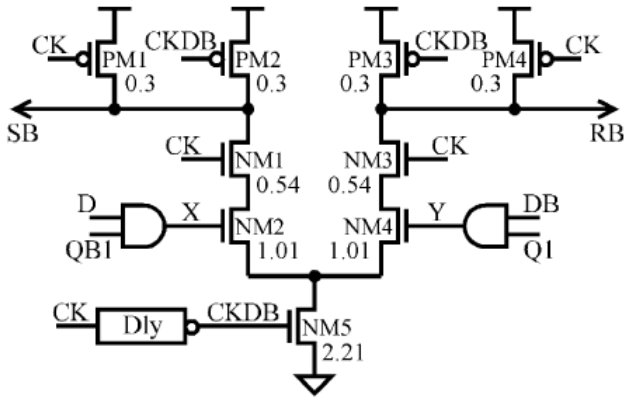

Figure 5 : Conditional Data Mapping Flip Flop

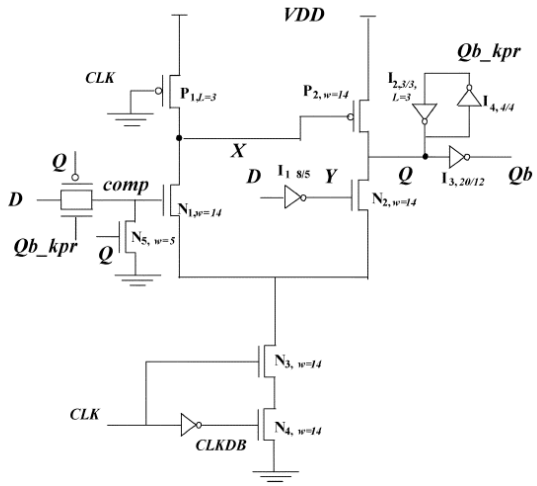

Figure 6: Clocked Pair Shared Flip Flop

IV. SIMULATION RESULTS

The simulation results for above types of flip flops were obtained from HSPICE simulations in 180nm CMOS technology at room temperature. VDD is 1.8 V. The parasitic capacitances were extracted from the layouts. The setup used in our simulations is shown in Fig 7. In order to obtain accurate results, we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the output is required to drive an output load. An inverter is placed after output, providing protection from direct noise coupling.

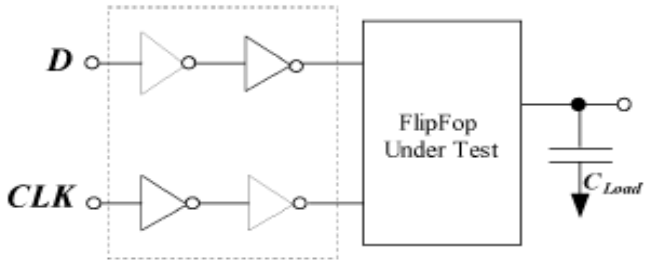

Figure 7: Setup used for our Simulations

Each design is simulated using the circuit at the layout level. All capacitances were extracted from layout such that we can simulate the circuit more accurately. This is because the internal gate capacitance, parasitic capacitance, and wiring capacitance affect the power consumption heavily in deep sub micrometer technology. Further the delay strongly depends on these capacitors.

Circuits were optimized for power delay product (PDP)[15]. Delay is data to output delay (D-to-Q delay) which is the sum of the setup time and the clock to the output delay. The D-to-Q delay is obtained by sweeping the high to low and low to high data transition times

with respect to the clock edge and the minimum data-to-output delay corresponding to optimum set up time is recorded.

Power consumed in the data and clock drivers are measured in our simulation[15]. In this way, the load seen by driving logic imposed by the flip-flop is included in total power consumption. The clock power is the power consumed by the clocked transistors. Fig 8, 9 shows power consumption versus no of transistors and no of clk transistors respectively. It is a very important parameter since it determines potential power saving in the clock distribution network by reducing the clock load. CPSFF leads to about 40% reduction in number of clocked transistor. It achieves 24% less clock driving power which improves power efficiency considerably. CPSFF improves overall power consumption about 9%.

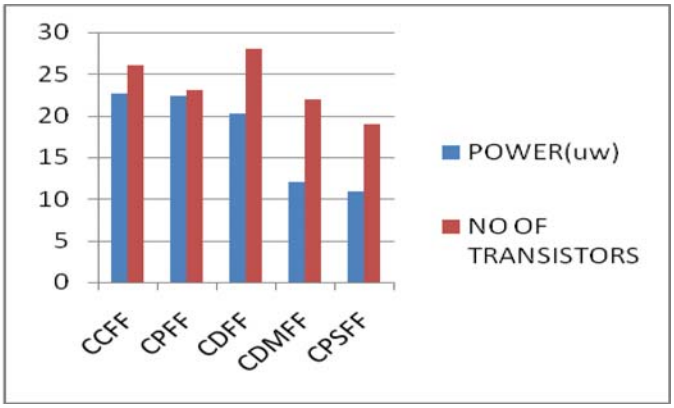

Figure 8: Power Breakdown VS Transistors

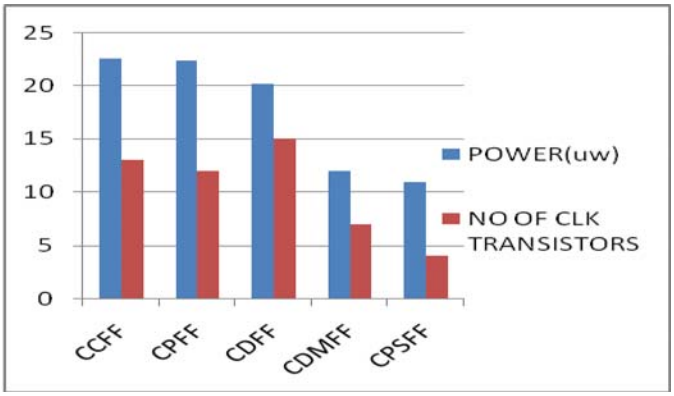

Figure 9: Power Breakdown VS CLK Transistors

Table I

Comparing the Flip-Flop in terms of Delay, Power and Power Delay Product

Flip Flops	No. of Transistors	No of Clock Transistors	DQ (pS)	P (uw)	PDP (fJ)
CCFF	26	13	206	22.6	4.66
CPFF	23	12	189.2	22.4	4.24
CDFF	28	15	185	20.2	3.74
CDMFF	22	7	389	11.98	4.63
CPSFF	19	4	392	10.9	4.28

From the charts, we have noticed that if the flip-flop is not in the stable operating region, its delay will dominate the PDP. We might further notice that PDP trends for stable regions of operations and across frequencies is a fair comparison. We also observe that the trending is similar to the maximum power trend.

V. CONCLUSION

We conclude this paper by outlining an important set of guidelines which are the corner-stone for low power flip-flop design methodology and low power flip-flop simulation .In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits. Our experimental results enabled us to identify the power and performance trade-offs of existing flip-flop designs.

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